AMENDMENT TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1 to 27. (Canceled).

28. (Currently Amended) An instruction pipeline in a microprocessor, comprising:

a plurality of pipeline units, each of the pipeline units configured to process instructions, wherein:

the instructions are distributed in multiple threads for the plurality of pipeline units to process; and

at least one of the plurality of pipeline units is configured to:

receive an instruction the instructions from another of the pipeline units;

issue the received instruction to a downstream pipeline unit; [[and]]

store [[the]] a copy of the received instruction; instructions, wherein the instructions are distributed in multiple threads for the plurality of pipeline units to process and

the at least one of the plurality of pipeline units is configured to subsequent to the issuing of the received instruction, issue reissue to the [[a]] downstream pipeline unit the copy of the received instruction at least one of the instructions in one of the multiple threads after a stall occurs in the one of the multiple threads, the reissued at least one of the instructions having been previously issued to the downstream pipeline unit.

29. (Currently Amended) An instruction pipeline in a microprocessor, comprising:

at least one upstream pipeline unit configured to issue each of a series of instructions on one of a plurality of instruction threads;

at least one downstream pipeline unit configured to allocate each of the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions were issued; and

an instruction queue, wherein in a first operating mode, the instruction queue is [[being]] configured to pass each of the series of instructions from the at least one upstream pipeline unit to the at least one downstream pipeline unit on the one of the plurality of

instruction threads on which each of the series of instructions were issued and configured to store <u>a copy of</u> each of the series of instructions, at least one memory location being dedicated to each of the plurality of instruction threads, and in a second operating mode the instruction queue <u>is</u> configured to <u>issue</u> ~~reissue~~ to the at least one downstream pipeline unit at least one of the <u>copies</u> ~~series of instructions~~ on the one of the plurality of instruction threads on which <u>a corresponding</u> [[the]] at least one of the series of instructions was <u>previously</u> issued.

      30. (Currently Amended) The instruction pipeline of claim 29, wherein the instruction queue in the first operating mode is configured to alternate passing the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions were issued when a stall signal is not present on any of the plurality of instruction threads, and when the stall signal is present on one of the plurality of instruction threads, the instruction queue is configured to <u>pass</u> ~~issue~~ the series of instructions on an other one of the plurality of instruction threads.

      31. (Previously Presented) The instruction pipeline of claim 29, wherein the at least one upstream pipeline unit is configured to determine the one of the plurality of instruction threads on which to issue each of the series of instructions based the availability of resources on each of the plurality of instruction threads.

      32. (Currently Amended) A method of processing instructions in a multi-threaded instruction pipeline, comprising:
      issuing, from an upstream pipeline unit, <u>original</u> instructions on one of a plurality of instruction threads;
      storing <u>a copy of each of</u> the issued <u>original</u> instructions in a queue, and passing the issued <u>original</u> instructions to a downstream unit on the one of the plurality of instruction threads;
      detecting a stall in the one of the plurality of instruction threads; and
      after detecting the stall, <u>issuing at least one of the copies</u> ~~reissuing at least one of the issued instructions~~ from the queue, on the one of the plurality of instruction threads on which the instructions were issued.

33. (Currently Amended) The method according to claim 32, further comprising:

maintaining a respective pointer for each of the plurality of instruction threads, wherein the ~~reissuing~~ step of issuing the at least one copy includes issuing ~~reissuing~~ the at least one of the copies ~~issued instruction~~ from the queue using the respective pointer for the one of the plurality of instruction threads on which the original instruction was issued.

34. (Currently Amended) The method according to claim 32, further comprising:

alternating the issuance of original instructions between each of the plurality of instruction threads.

35. (Currently Amended) The method according to claim 32, further comprising:

selecting one of the plurality of instruction threads on which to issue the original instructions based on an availability of resources.

36. (Currently Amended) A microprocessor, comprising:

a multi-threaded instruction pipeline including:

at least one upstream pipeline unit configured to issue an instruction ~~instructions~~ on a selected one of a plurality of threads of the pipeline[[,]];

a downstream pipeline unit; and

an instruction queue configured to receive the instruction from the upstream pipeline unit, pass the received instruction ~~issued instructions~~ to a downstream pipeline unit on the selected one of the plurality of threads, and store a copy of the received instruction ~~issued instructions~~, the instruction queue further configured to transmit ~~reissue~~, on the selected one of the plurality of threads, the copy of the received instruction ~~at least one of the stored instructions~~ in an event of a downstream stall on the selected one of the plurality of threads.

37. (Previously Presented) The microprocessor according to claim 36, wherein the at least one upstream pipeline unit includes at least one of a trace cache and a micro-instruction sequencer.

38. (Previously Presented) The microprocessor according to claim 36, wherein the downstream pipeline unit includes an execution unit.

39. (Previously Presented)   The microprocessor according to claim 36, wherein the instruction queue is configured to select one of the threads based on available resources.

40. (Currently Amended)   The microprocessor according to claim 36, wherein the instruction queue is configured to alternate between the plurality of threads when passing [[the]] instructions.

41. (Previously Presented)   The microprocessor according to claim 36, wherein the instruction queue is configured to pass instructions on one of the threads, and configured to switch to a different one of the threads when a stall is detected on the one of the threads.

42. (Currently Amended)   The microprocessor according to claim 36, wherein the instruction queue includes:

a memory device to store copies of received [[the]] instructions; and

an output multiplexer which is configured, in a first mode of operation, to pass the received instructions from the upstream pipeline unit to the downstream pipeline unit, and which is configured, in a second mode of operation, to issue reissue the at least one of the stored instruction copies instructions.